electrically connecting a channel layer located in a part of the island-like semiconductor layer opposed to the gate electrode to a channel layer of the memory cell is further formed between the control gate and the gate electrode.

A2 Concl'd

15. (Amended) A semiconductor memory according to claim 9, wherein all, some or one control gate(s) are formed of the same material as all, some or one gate electrode(s).

16. (Amended) A semiconductor memory according to claim 9, wherein the charge storage layer and the gate electrode are formed of the same material.

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23. (Amended) A process according to claim 20, wherein the introduced impurity is diffused so that a continuous impurity diffusion layer is formed in the island-like semiconductor layer in a direction horizontal to a surface of the semiconductor substrate.

24. (Amended) A process according to claim 20, wherein a plurality of island-like semiconductor layers are formed in matrix, sidewalls of the island-like semiconductor layers are oxidized to form oxide films, and the oxide films are removed so that the width of the island-like semiconductor layers in one direction is smaller than a distance between the island-like semiconductor layers in the same direction.

25. (Amended) A process according to claim 20, wherein a third conductive film is formed between separated first conductive films.

26. (Amended) A process according to claim 20, wherein the first conductive film is separated into two or more separated first conductive films which are located so closely that a channel layer formed beneath a separated first conductive film along the island-like semiconductor layer is electrically connected to an adjacent channel layer.

27. (Amended) A process according to claim 20, wherein an insulating film is formed in a part of a surface of the island-like semiconductor layer, another insulating film is formed in another